Notice of Allowability	Application No.	Applicant(s)	
	10/711,748	CHATTY ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/09/06*.

2. ☒ The allowed claim(s) is/are *1, 4 - 11*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on November 9, 2006. Claims 2, 3 and 12 - 20 are deleted; Claim 1 is amended. Amendment and arguments have overcome rejections under 102 (b) and 103(a).

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney, Mr. Mueller on November 28, 2006.

1. Please amend Claim 1, line 6 as follows, after "voltage source" add: -- whereby at least one of the transistors is biased into an at least a partially on-state during normal operation of the chip;" --

2. Please amend Claim 4, line 3 as follows, change " a bias" to --"a resistive bias"--

3. Please amend Claim 7, line 5 as follows, after "prescribed value" add: --"whereby at least one of the upper and lower nFET are biased into an at least a partially on-state during normal operation;" --

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 1 discloses a power clamp for integrated circuit for ESD protection including following elements: a transistor network composed of a first nFET and a second nFET respectfully connected in series with one another between a voltage source and a ground, and a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground; a bias network configured to bias a gate of the first transistor of the transistor network to a portion of a voltage value of the voltage source, whereby at least one of the transistors is biased into at least a partially on-state during normal operation of the chip; and a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of the second transistor of the transistor network.

The closest reference for the claim is Drapkin et al. (US 6,459,553), which discloses a transistor network including three series connected transistor between a voltage source and a ground (210, 212, 214 in Fig. 4), a bias network (204 and 202 in Fig. 4) configured to bias a gate of a first transistor (210 in Fig. 4) to a portion of a voltage value of the voltage source, and a trigger network (132, 134 in Fig. 4) communicating the occurrence of an electrostatic discharge to the gate of the second transistor (214 in Fig. 4). However, it does not disclose at least one of the transistors being biased into at least a partially on - state during normal operation of the chip, as required by Claim 1. The same limitation is recited over again in another independent Claim 7, thus making it allowable.

As per independent Claim 4, it recites, inter alia, a resistive divider configured to bias a gate of a first transistor. The reference recites the divider composed of diodes

(220a, 220b, 220c, 220d in Fig. 4), with specific requirement to their diffusion areas to ensure that during ESD event the upper transistor is on. The resistive divider of the Application being conducting small current all the time and holding the upper transistor in partially on - state makes such arrangement unnecessary.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
11/29/2006

BRIAN SIRCUS
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